

## Case study: Compression PoC for Nokia proves 40x performance improvement

### NOKIA

#### Industry pain points

While virtualization brings a series of obvious benefits, it also introduces new hurdles. The huge flexibility made possible by software (SW) must inevitably be weighed against the large consumption of resources required to deliver a performance level that matches hardware (HW). For SW compression, one issue is that the widely applied gzip format is overly CPU intensive. This imposes substantial speed limitations and drops the overall application performance.

#### Client challenge

Nokia is a global leader in creating technologies at the heart of the connected world, from enabling infrastructure for 5G and the Internet of Things, to emerging applications in virtual reality.

When Nokia encountered a performance bottleneck related to the SW file compression of their storage application, they wanted to explore a HW acceleration solution to compress and store 40 Gbps of raw data. This needed to happen on the fly, exploiting only a minimum of CPU

resources. Napatech was engaged to develop the Proof of Concept (PoC).

*“The PoC showed excellent results and truly underpinned Napatech’s dexterity in the virtualization sphere.”*

Jari Ruohonen  
Sr. Product Manager, Nokia Airframe Group

#### Our solution

To help Nokia unburden their CPUs, Napatech designed a compression acceleration solution based on a Napatech SmartNIC, powered by FPGA. With this solution, the raw data would be sent seamlessly from the application to the HW accelerated compression engine running on the SmartNIC. An advanced queueing system ensured that multiple compression tasks could be performed simultaneously. After compression, the file would be returned to the application with a selection of headers - gzip or similar - readable to the relevant SW. Next, the compressed file could be offloaded for storage.

#### Challenge

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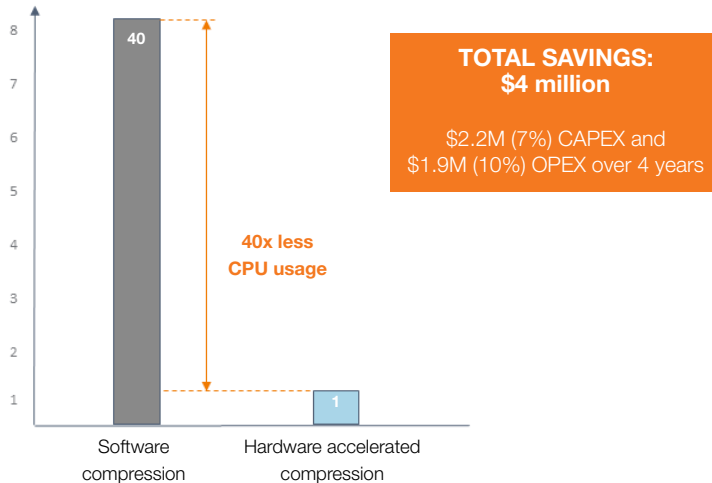
#### Solution

To help Nokia unburden their CPUs, Napatech designed a compression acceleration solution based on a Napatech SmartNIC, powered by FPGA.

#### Benefits

Results were outstanding: the HW acceleration demonstrated 30x faster compression time and 40 Gbps sustained file compression for storage, using only 1 CPU core - a massive performance improvement with estimated CAPEX and OPEX savings of around \$4 million in just four years’ time.

## Improved performance with hardware acceleration



### Benefits

The performance improvements achieved with this solution were stunning: 30 times faster compression time and 40 Gbps sustained file compression for storage using only 1 CPU core. In contrast to the 40 cores utilized to achieve the same performance in SW only, these figures were outstanding.

With this solution in place, the data compression could be performed quickly and reliably – losing no information, even at high speeds. Over a period of four years, the CPU optimization compared to SW was estimated to generate CAPEX and OPEX savings of around \$4 million for a data center with approx. 10,000 servers.

### Solution highlights:

- 40 Gbps sustained file compression/decompression for storage
- Only 1 CPU core used vs. 40 cores for SW only
- 40x improvement vs. SW compression
- 30x faster compression time
- High compression ratio typically up to 3:1
- Unique de-duplication ID per file

### Napatech

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We enhance open and standard virtualized servers to boost innovation and release valuable computing resources that improve services and increase revenue.

Our Reconfigurable Computing Platform™ is based on a broad set of FPGA software for leading IT compute, network and security applications that are supported on a wide array of FPGA hardware designs.

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### EUROPE, MIDDLE EAST AND AFRICA

Napatech A/S  
Copenhagen, Denmark

Tel. +45 4596 1500  
info@napatech.com  
www.napatech.com

### NORTH AMERICA

Napatech inc.  
Boston, Massachusetts  
Los Altos, California  
Washington D.C.

Tel. +1 888 318 8288  
info@napatech.com  
www.napatech.com

### APAC

Napatech China/South Asia  
Taipei City, Taiwan  
Tel. +886 2 28164533 Ext. 319

Napatech Japan K.K.  
Tokyo, Japan  
Tel. +81 3 5326 3374

ntapacsales@napatech.com  
www.napatech.com