SOLUTION DESCRIPTION

NAPATECH VIRTUALIZATION SOLUTION FOR HARDWARE OFFLOAD

NAPATECH VIRTUALIZATION SOLUTION FOR HARDWARE OFFLOAD

The following document provides a description of the Napatech Virtualization Solution for Hardware Offload. Designed specifically for NFV use cases, the Napatech SmartNIC offloads common compute-intensive data processing functions that would otherwise require an unacceptable number of server CPU resources to function efficiently.

THE HARDWARE OFFLOAD SOLUTION – HOW DOES IT WORK

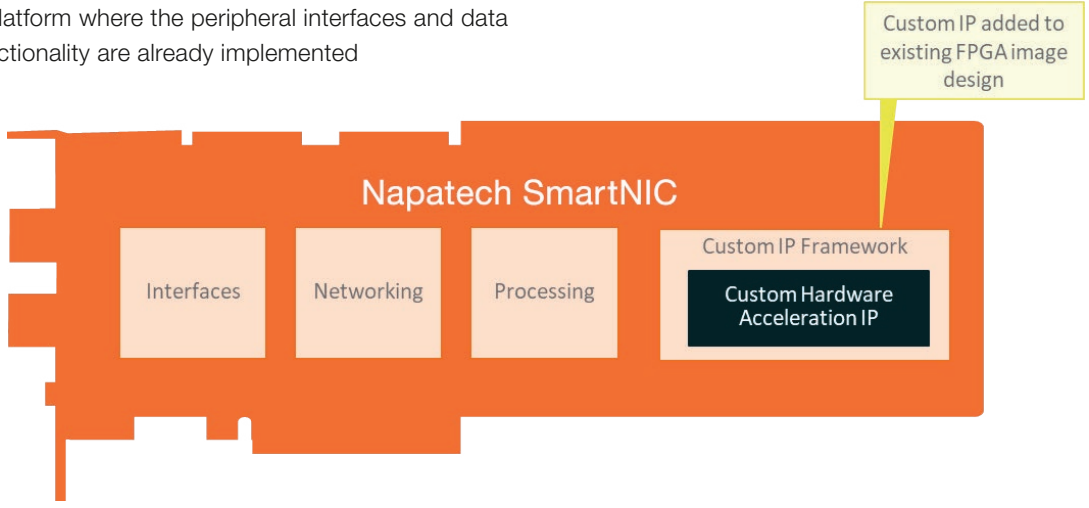
Using a partial reconfiguration approach, the Hardware Offload Solution allows any 3rd party Intellectual Property (IP) function block to be added to the FPGA on the Napatech SmartNIC. This includes IP blocks from independent vendors for functions such as encryption, compression and transcoding, but also includes IP blocks developed by customers, when there is a need to keep the contents of the IP block confidential. Examples of the latter could be special algorithms or other in-house developed technology.

When developing solutions based on FPGA technology, the most difficult and time consuming task is to implement peripheral interfaces with an acceptable level of performance, especially at high speeds. The Hardware Offload Solution provides a platform where the peripheral interfaces and data handling functionality are already implemented providing a significant time and cost advantage. This includes interfaces to on-board memory, the server PCIe bus interface and interfaces to physical ports (if required). This solution can also be combined with the Napatech OVS Acceleration Solution to enable a combined data delivery and processing offload solution on the same SmartNIC.

The FPGA framework ensures that there is no interference between the Napatech peripheral interfaces and additional functionality, such as OVS Acceleration, and the IP block. Only 30% of the FPGA resources are consumed by the Napatech framework including the OVS Acceleration logic with the remainder of the FPGA logic available to the IP block to be inserted.

THE BENEFIT FOR THE CUSTOMER

There are two levels of benefit to the customer; the benefit of significant performance improvement by offloading CPU-intensive data processing tasks and the benefit of faster time-to-market with lower cost of using an FPGA-based hardware offload solution with pre-integrated and tested peripheral interfaces.

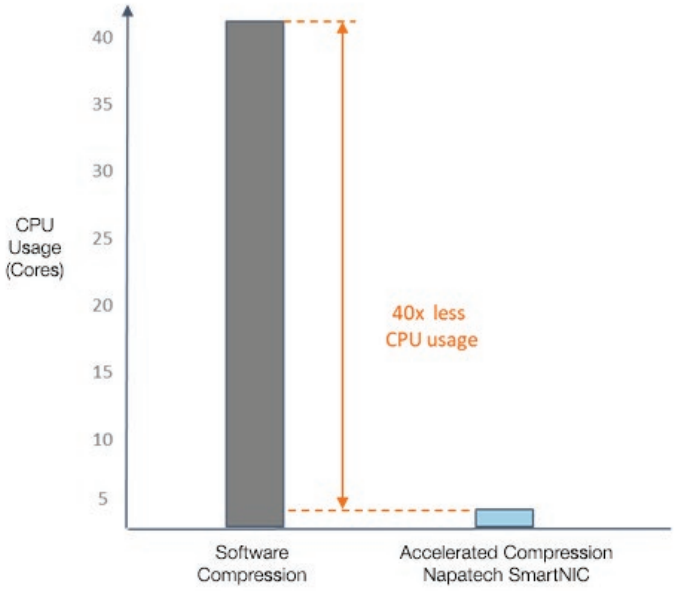


Since the solution is based on an FPGA design, customers can benefit from the fact that there is a broad ecosystem of IP block vendors supporting major FPGA vendor tools and environments. This allows the best-in-breed IP block to be selected for each specific task with the ability to "drop-in" and replace this block on a needs basis.

An additional benefit of the solution is that it can be used as either a co-processor focused on offloading a specific function, such as encryption or compression or it can be combined with the data delivery solution with the data processing applied as data enters and leaves the server.

TESTS AND PERFORMANCE NUMBERS

To illustrate the performance of the Hardware Offload Solution, we will refer to a 40G data file compression PoC that was developed for Nokia (see https://www.napatech.com/support/resources/case-studies/compression-poc-for-nokia-proves-40x-performance-improvement/). The performance figures shown below provide an indication of the significant advantages of offloading compute-intensive functions to deterministic processing platforms, such as FPGAs.



For this particular case, it was possible to perform file compression at a speed of 40 Gbps using just one CPU core to manage the offload and direction of the file to be compressed. This was a 40 times improvement compared to performing the compression in software as a single core can only process 1 Gbps of data. Similar performance has also been seen for functions such as encryption where 40 Gbps encryption can be performed using a single core compared to 40 cores for a software encryption solution.

WORKING WITH THE HARDWARE OFFLOAD SOLUTION

To take advantage of the Hardware Offload Solution, users need to use a Napatech SmartNIC to ensure best performance. The interfaces from the IP blocks to the FPGA framework delivered by Napatech are based on standard interfaces typically provided by IP block vendors, which are designed to support isolation and performance. The interface to the virtual application is specific to the IP block being used.

POWERFUL AND FLEXIBLE HARDWARE OFFLOAD SOLUTION THAT SIGNIFICANTLY ACCELERATES TIME-TO-MARKET

The Napatech Virtualization Solution for Hardware Offload provides a compelling alternative to solutions based on proprietary hardware as well as a faster time-to-market compared to developing an in-house FPGA-based offload solution without having to compromise on flexibility or performance.

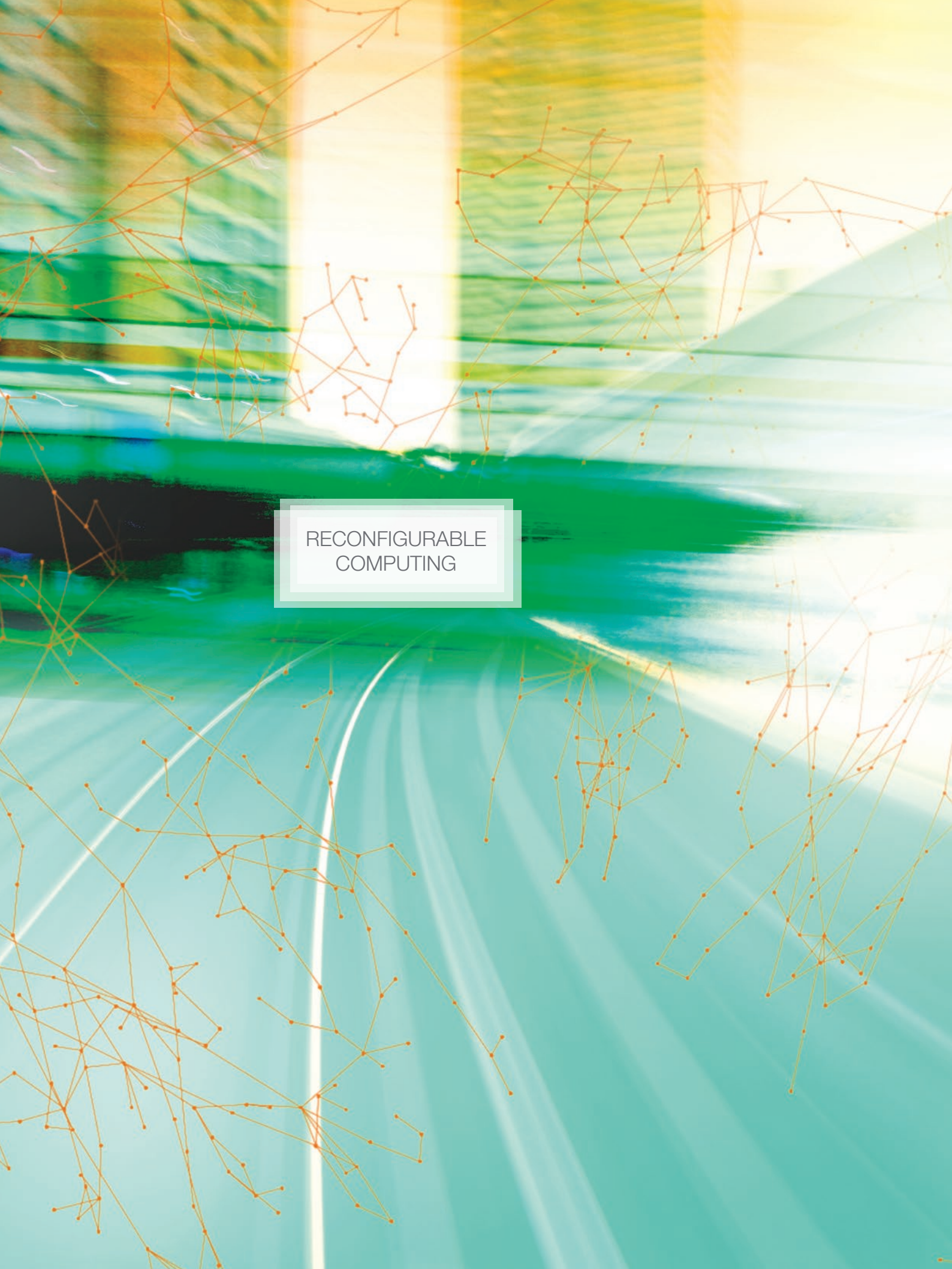
For more information see our website:
www.napatech.com/solutions/virtualization-solutions

Or contact Napatech for more information:
www.napatech.com/contact

COMPANY PROFILE

Napatech helps companies to reimagine their business, by bringing hyper-scale computing benefits to IT organizations of every size. We enhance open and standard virtualized servers to boost innovation and release valuable computing resources that improve services and increase revenue.

Our Reconfigurable Computing Platform™ is based on a broad set of FPGA software for leading IT compute, network and security applications that are supported on a wide array of FPGA hardware designs.


RECONFIGURABLE
COMPUTING

EUROPE, MIDDLE EAST AND AFRICA
Napatech A/S
Copenhagen, Denmark

Tel. +45 4596 1500
Info@napatech.com
www.napatech.com

NORTH AMERICA
Napatech Inc.
Boston, Massachusetts
Los Altos, California
Washington D.C.
USA

Tel. +1 888 318 8288
Info@napatech.com
www.napatech.com

APAC
Napatech Japan K.K.
Tokyo, Japan
Tel. +81 3 5326 3374

ntapacsales@napatech.com
www.napatech.com

DN-1117 Rev.3