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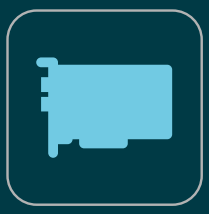
RECONFIGURABLE COMPUTING



Napatech SmartNICs

SOLUTION DESCRIPTION

Powerful Test & Measurement up to 100G Line Rate

For Napatech FPGA-based SmartNICs

Solution:
Build advanced Test & Measurement solutions with COTS servers and Napatech FPGA SmartNIC's
The Napatech Link Capture software supports powerful features for Test & Measurement applications.

Nanosecond hardware transmit and receive timestamping enables precision network roundtrip delay and jitter measurements.

Napatech Link Capture software supports an advanced scheme for L2 and L3/L4 (IP/TCP/UDP) Tx checksums generation and Rx checksum verification.

All of this is supported for 10G, 25G, 40G and 100G network speeds.

Key Benefits
- Napatech FPGA-based SmartNICs include specialized and powerful test and measurement features on standard COTS servers, outperforming a standard NIC
- Precision hardware time stamping measurements
- For each transmitted packet, the application can control individually how checksums are generated, offering a flexible setup
- Napatech guarantees line rate receive and transmit and full throughput with zero packet loss for all packet sizes

Use case:
Roundtrip latency measurement in communication networks
In roundtrip latency measurement it is critical to provide a precise time stamp for both transmitted and received packets. Generation of checksums is a burden to the application, and risks overloading the CPUs. Overloading the CPUs affects the overall system performance, particularly in 40G or 100G networks.

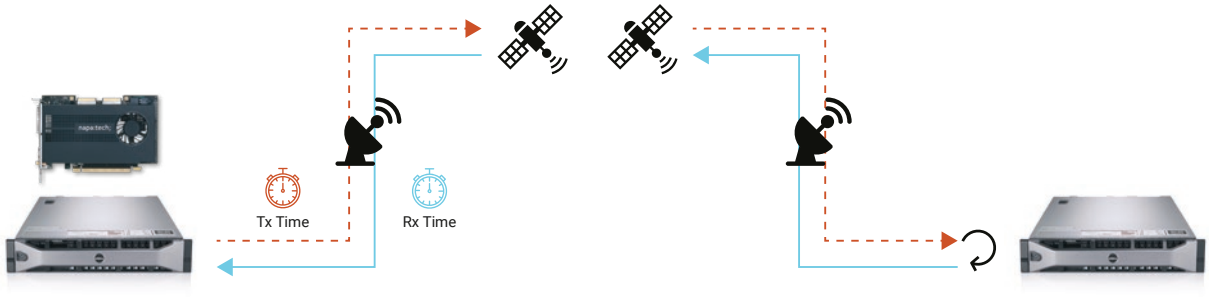
To address the challenges of roundtrip latency measurement, the Napatech SmartNICs provide:

- High-precision start-of-frame or end-of-frame Tx/Rx time stamps, sampled with 1 nanosecond resolution
- L3/L4 checksum generation and verification for latency measurements across routed networks
- Generate invalid L2/L3/L4 checksums for error simulation
- Per packet inter-frame gap control for jitter simulation

Use Case:
Replay captured traffic for troubleshooting or simulation
A major challenge in existing packet capture systems is the performance demands of precision capture and replay. Not only time stamp precision is a challenge, but also the heavy load on the CPUs can be an issue. Furthermore, performance degradation may be noticed when testing traffic bursts at full throughput, for example, the risk of packet loss and lack of replay precision including packet bursts.

To solve these capture-replay challenges Napatech SmartNICs provide:

- Replaying traffic precisely as captured including exact timing, and replay even with errors
- Error simulation by generating packets with invalid checksums



- Flexible checksum generation and verification, enabling e.g. replay with modified IP addresses or port numbers
- The speed of the replay can be adjusted to simulate e.g. burst behavior. The replay may either be faster or slower than the captured traffic. The transmit time stamp per packet can be controlled by the application.

Use Case:
Traffic Generation
In traffic generation systems the packets must be transmitted and received with time stamp precision. In addition software-based traffic generation solutions heavily load the CPUs, affecting the overall system performance.

High-speed full throughput, including the maximum theoretical burst, must be guaranteed, for packet receive and packet transmit.

For traffic generation Napatech SmartNICs provide:

- Accelerated traffic generation solutions, for example using the open source TRex traffic generator
- Checksum generation and checksum verification
- Applying time stamp injection in hardware

Selected Features
HW Time-Stamping
- 1 ns time stamp resolution
- Rx time stamp
- Tx time stamp inject

Tx Time stamp inject
- Application controlled action per packet
- Tx time stamp insertion at offset relative to L3/L4 headers
- 8-byte time stamp + 2 bytes for L3/L4 checksum compensation (used in combination with L3/L4 Tx checksums generation)

L2 and L3/L4 (IP/TCP/UDP) Tx checksums generation
- Application controlled action per packet
- Generate correct checksum
- Generate incorrect checksum
- Leave checksum unchanged

L2 and L3/L4 (IP/TCP/UDP) Rx checksums verification
- Valid/invalid indication in packet descriptor and via API
- Filtering on valid/invalid checksums

See Product Overview and the documentation for a complete feature list.

Napatech Link™ Capture Software
Napatech Link™ Capture Software supports a broad range of applications and use cases. Where standard Network Interface Cards (NICs) suffer from intolerable packet loss for the target applications, Napatech guarantees line rate throughput with zero packet loss and replay for all packet sizes.

Key Features
- Zero packet loss under all conditions
- Full throughput up to 100 Gbps bi-directional
- Nanosecond timestamping and packet merge
- 50 million flows with stateful match/action
- Flow records with metrics for both directions
- PCAP and DPDK API support

Napatech SmartNICs
Napatech is the pioneer and preferred supplier of FPGA-based SmartNICs designed to improve application performance and provide ultimate network flexibility and security. Our industry-leading feature set provides capabilities that are crucial for high-speed, real-time data processing.

With Napatech SmartNICs, you can build affordable, high-performance solutions based on standard, low-cost servers. The card offers market-leading integration capabilities and provides a robust and well-documented Application Programming Interface (API) that seamlessly integrates with open source, custom-developed or commercial applications.

DN-1263 Rev. 1

Napatech helps companies to reimagine their business by bringing hyperscale computing benefits to IT organizations of every size. We enhance open and standard virtualized servers to boost innovation and release valuable computing resources that improve services and increase revenue. Our Reconfigurable Computing Platform™ is based on a broad set of FPGA software for leading IT compute, network and security applications that are supported on a wide array of FPGA hardware designs.